

FinFETs (Fin Field Effect Transistors)

Abstract

A FinFET structure that prevents parasitic electrical leakages between its gate region and its fin region and between its gate region and its epitaxial region (source/drain regions). The structure is formed by first forming a fin region on top of an electrically insulating layer. Next, a gate stack having gate spacers thereon is formed on top of and electrically insulated from the fin region. Then, the final S/D (source/drain) regions are formed by epitaxially growing a semiconductor material from the two ends of the fin region not covered by the gate stack. Next, another electrically insulating layer is formed on top of the structure except the gate spacers. Next, the gate spacers and portions of the gate stack beneath them are replaced with a dielectric material.